

11/27/02 2811 #  
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Shen Examiner: N. Parekh  
Serial No.: 09/407204 Group Art Unit: 2811  
Filed: September 28, 1999 Docket: 08688.0128US01  
Confirmation No.: 2434 Notice of Allow. N/A  
Date:  
Due Date: November 25, 2002  
Title: SEMICONDUCTOR CHIP MODULE



CERTIFICATE UNDER 37 CFR 1.10:

"Express Mail" mailing label number: EV037622825US  
Date of Deposit: November 25, 2002

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By:   
Name: John Junkers

Commissioner for Patents  
Washington, D.C. 20231

Sir:

We are transmitting herewith the attached:

- ☒ Return postcard
- ☒ Transmittal Sheet in duplicate containing Certificate of Mailing
- ☒ Amendment Including Version With Markings To Show Changes Made
- ☒ Small entity status has been previously established
- ☒ Request for Extension of Time for 1 month(s) and fee of \$55.00

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Please consider this a PETITION FOR EXTENSION OF TIME for a sufficient number of months to enter these papers or any future reply, if appropriate. Please charge any additional fees or credit overpayment to Deposit Account No. 13-2725. A duplicate of this sheet is enclosed.

3200 IDS Center  
80 South Eighth Street  
Minneapolis, Minnesota 55402-2215  
USA  
(612) 332-5300

By:   
Name: Bryan A. Wong  
Reg. No.: 50,836  
MDS:BAW/tlp



#20/B  
12.10.02  
PATENT *Muller*

S/N 09/407204

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

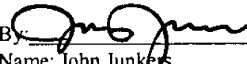
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By:   
Name: John Junkes

AMENDMENT UNDER 37 C.F.R. §1.111

Commissioner for Patents  
Washington, D.C. 20231



Dear Sir:

In response to the Office Action dated July 25, 2002, with the time for response extended with a one month extension of time from October 25, 2002 to November 25, 2002, please amend the above referenced patent application as indicated herein.

In the Claims

Please amend the claims as follows. The claims are amended in accordance with 37 C.F.R. §1.121. No new matter has been added.

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- B<sup>1</sup>
1. (Amended) A semiconductor chip module comprising:  
a chip-mounting member having opposite first and second surfaces, a set of first circuit traces, and a plurality of plated through holes that extend through said first and second surfaces and that are connected to said first circuit traces;  
a first semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;